A VLSI MODEL OF RANGE-TUNED NEURONS IN THE BAT ECHOLOCATION SYSTEM

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ABSTRACT

The neural computations that support bat echolocation are of great interest to both neuroscientists and engineers, due to the complex and extremely time-constrained nature of the problem and its potential for application to engineered systems. In various areas of the bat's brain, there exist neural circuits that are sensitive to the specific difference in time between the outgoing sonar vocalization and the returning echo, or time-of-flight. While some of the details of the neural mechanisms are known to be species-specific, a basic model of re-afference triggered, post-inhibitory rebound timing is reasonably well supported by the available data. We have designed low-power neuromorphic VLSI circuits to mimic this mechanism and have demonstrated range-dependent outputs for use in a real time sonar system. These circuits are being used to implement range-dependent vocalization rates and amplitudes.

1. INTRODUCTION

Information about target range has many uses for bats during both prey-capture and navigation tasks. Beyond the extraction of target distance and velocity, it may be important for less obvious tasks, such as optimizing the parameters of the echolocation process. As a bat approaches a target, it alters many parameters of its vocalization, including pulse repetition rate, pulse duration, spectral content, and amplitude [1].

Neurons have been found in bats that show a selective response to paired sounds (simulated vocalization and echo) presented at particular delays. The cells' responses to the delayed sounds are much greater than the sum of the responses to the individual sounds presented alone. These neurons are referred to as delay-tuned cells and are found in many levels of the bat brain [2][3][4]. Disruption of cortical delay-tuned cells has been shown to impair a bat's ability to discriminate between artificial pulse-echo pairs with different delays [5].

The largest amount of information related to the mechanisms underlying delay-tuning comes from the mustached bat, *Pteronotus parnellii* [2][6][7][8][9][10][11][12]. In this species, delay-tuned cells respond specifically to the first harmonic of the echolocation call (FM_1) paired with a delayed higher harmonic (FM_{2-4}) [13]. In contrast, delay-tuned cells in the big brown bat, *Eptesicus fuscus* respond preferentially to an initial loud sound followed by a delayed softer sound [14]. These patterns of response are thought to relate to the discrimination between the outgoing vocalization and the returning echo. In the case of *Pteronotus*, the first harmonic of the vocalization is weak, and is probably too attenuated in returning echoes to impact the ranging system. For *Eptesicus*, the outgoing vocalization is obviously much louder than the returning echoes. Note, however, that in both cases the timing is started by the sound of the outgoing pulse, and not an internal trigger.

The earliest point in the auditory pathway where delay-tuned cells have been found is in the inferior colliculus (IC) of *Pteronotus* [2], and it is hypothesized that this is where the delay-tuned responses are formed. When presented with FM_1 tones, IC delay-tuned cells either do not respond at all, or respond weakly at latencies as long as 30ms [10]. In response to FM_n tones, the cells respond weakly with consistent short latencies [10]. In response to paired FM_1-FM_n sounds, IC delay-tuned cells have tuning curves similar to figure 1. The delay eliciting the maximum response in delay-tuned cells is called the best delay (BD) and is highly correlated with the latency of the response to FM_1 tones [10]. This leads to a latency-coincidence hypothesis for delay tuning, in which the cell's facilitated response at long delays is due to the coincidence of the long latency FM_1 response and the short latency FM_n response [3][10].

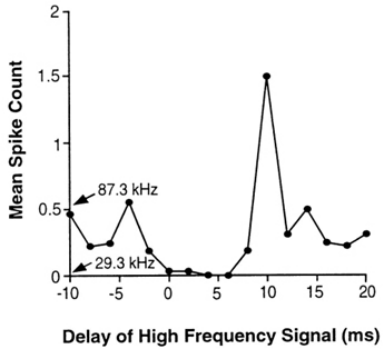

Figure 1. From Portfors and Wenstrup (1999). Tuning curve of a delay-tuned neuron in mustached bat IC. Average number of spikes is plotted vs. the time interval between the FM_1 (29.3 kHz) and FM_n (87.3 kHz) presentations. Arrows indicate the average number of spikes in response to each stimulus presented alone

An interesting question is how delay-tuned cells can have such long latency responses to the FM_1 sounds. It is unlikely that the short neural pathways from the cochlear nucleus to IC could create

such long latencies. In Figure 1, there is a clear period of suppressed response beginning at 0ms delay. This suppression is consistent with a period of inhibition triggered by the FM_1 harmonic and lasting until the time of facilitation. This has led to the proposal of a post-inhibitory-rebound (PIR) mechanism for generating long-latency responses and facilitation [15].

In the PIR model for delay-tuning, the outgoing vocalization triggers a long lasting inhibition in delay-tuned cells. At the offset of inhibition, an instability in the membrane dynamics of the delay-tuned neuron leads to a brief excitatory jump above resting potential. If excitatory input from a returning echo coincides with this rebound event, the membrane potential will cross threshold, and the cell will spike. This model predicts that blocking of inhibition in the IC should reduce or eliminate the latency-coincident facilitation of delay-tuned cells. Results from a study by Wenstrup and Leroy [12] indicate that blocking the inhibitory transmitter glycine has such an effect. VNLLc, a lower brainstem area, which contains neurons that respond with short and remarkably precise latencies, has been shown to contain glycenergic cells which project to IC. [16]

2. VLSI CIRCUIT IMPLEMENTATION

2.1 Neuron Circuit

The design of our delay-tuned neuron is intended to capture the fundamental functional aspects of biological delay-tuned neurons while maintaining simplicity of use and maximum control over neuron behavior.

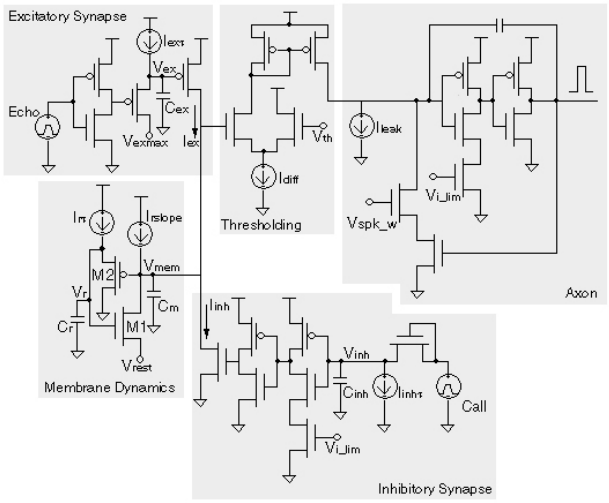

Figure 2. Circuit schematic for the rebound neuron. Thirteen neurons per chip were fabricated in an AMI 1.5µm process by MOSIS.

The analog processing components in the neuron are implemented using transistors operating in the subthreshold regime. For analysis, we assume transistors are operating in saturation, and the drain current can be computed as:

for the nFET, $$I_{dn} = I_0 e^{\frac{\kappa_n V_{GB} - V_{SB}}{V_T}} \quad (1.1)$$

for the pFET $$I_{dp} = I_0 e^{\frac{\kappa_p V_{BG} - V_{BS}}{V_T}} \quad (1.2)$$

The delay-tuned neuron circuit is constructed from component circuits designed to mimic the basic elements of a PIR delay-tuned neuron. The circuit diagram for the neuron is shown in figure 2.

2.2 Inhibitory Synapse

Input spikes based on the outgoing vocalization trigger the inhibitory synapse, charging C_{inh} and driving V_{inh} to a high voltage, V_{inhH}. This signal is passed through a pair of inverters, activating an nFET that draws current from the membrane dynamics circuit, pulling V_{mem} to ground. $I_{inh\tau}$ discharges C_{inh} and the output nFET shuts down when V_{inh} drops below the switching point of the first inverter. The length of inhibition, which sets the best delay of the cell, is then given by:

$$t_{inh} = \frac{C_{inh}(V_{inhH} - V_{hl})}{I_{inh\tau}} \quad (1.3)$$

2.3 Membrane Dynamics

The membrane dynamics circuit generates post-inhibitory rebound in the cell, opening a facilitation window that leads to delay-tuning. In the absence of external input from the excitatory or inhibitory synapses, we can derive the equilibrium state of the membrane circuit. Applying the drain current equation to transistor M1, and solving for V_r, we obtain the equation:

$$V_{r\_eq} = \frac{1}{\kappa_n}\left(V_{rest} + V_T \ln\left(\frac{I_{rslope}}{I_0}\right)\right) \quad (1.4)$$

Following the same process for M2, and solving for V_{mem}, we obtain:

$$V_{mem\_eq} = \frac{1}{\kappa_p}\left(V_{r\_eq} - V_T \ln\left(\frac{I_{r\tau}}{I_0}\right)\right) + V_{dd}\left(1 - \frac{1}{\kappa_p}\right) \quad (1.5)$$

Substituting equation (1.4) into equation (1.5), and assuming the ideal case where $\kappa_n = \kappa_p = 1$:

$$V_{mem\_eq} = V_{rest} + V_T \ln\left(\frac{I_{rslope}}{I_{r\tau}}\right) \quad (1.6)$$

In the case where $I_{rslope} \le I_{r\tau}$, Transistor M1 will leave saturation and V_{mem} will sit slightly above V_{rest}.

The dynamic behavior of the circuit is best described in a stepwise manner. When an outgoing call triggers the inhibitory synapse, V_{mem} is pulled to ground, and V_r, which is connected to V_{mem} through a source follower, will also drop to some minimum voltage level, V_{r_min} which depends on $I_{r\tau}$.

On the release of inhibition, V_{mem} is less than V_{rest}, and the source and drain of M1 are reversed from the equilibrium state. Current flowing through M1 combined with I_{rslope} acts to drive V_{mem} very quickly toward V_{rest}.

It is reasonable to assume that with the appropriate biasing, V_{mem} will rise faster than V_r such that during the rebound, the current through M2 will be negligible, and V_r will rise at a rate of:

$$\dot{V}_r = \frac{I_{r\tau}}{C_r} \tag{1.7}$$

Under these conditions, once V_{mem} reaches V_{rest}, the current through M1 will be negligible, and V_{mem} will rise at a rate of:

$$\dot{V}_{mem} = \frac{I_{rslope}}{C_m} \tag{1.8}$$

V_{mem} will continue to rise at a linear rate, exceeding its equilibrium value, until V_r reaches V_{rest} and transistor M1 begins to turn on. The rebound will peak $\left(\dot{V}_{mem} = 0\right)$ when the drain current in M1 equals I_{rslope}, which occurs at the equilibrium voltage for V_r, given in equation (1.4). We define the duration of the rebound, t_{reb}, as the time interval after inhibition during which V_{mem} is rising. This is easily computed, provided that V_{mem} rises faster than V_r and the assumption that V_r rises linearly holds. The duration of the rebound is then:

$$t_{reb} = \frac{C_r\left(V_{r\_eq} - V_{r\_min}\right)}{I_{r\tau}} \tag{1.9}$$

An estimate for peak voltage of the rebound, V_{m_peak} can be obtained by assuming V_{mem} rises to V_{rest} nearly instantaneously, then applying the value of $\dot{V}_{mem}$ given in equation (1.8) and t_{reb}:

$$V_{m\_peak} = V_{rest} + \frac{I_{rslope}}{C_m} t_{reb} \tag{1.10}$$

The parameters of the circuit are adjusted so that V_{m_peak} is less than the neuron's voltage threshold.

The neuron will be most responsive to an excitatory current during the rising portion of the rebound. Normally, the active membrane properties dampen the response of the cell to excitatory currents. During the rebound period however, the active processes of the membrane have not recovered sufficiently to compensate for excitatory input. During this time window, I_{ex} sums with I_{rslope} to drive V_{mem}. $\dot{V}_{mem}$ can be computed as:

$$\dot{V}_{mem} = \frac{I_{ex} + I_{rslope}}{C_m} \tag{1.11}$$

In this condition, the current through M1 must compensate for I_{ex} + I_{rslope} before the membrane voltage peaks. If we assume a constant excitatory current, the rising time of the system, t_r, would be:

$$t_r = \frac{C_r\left(V_{rest} + V_T \ln\left(\frac{I_{ex} + I_{rslope}}{I_{r\tau}}\right) + V_{dd}(\kappa_p - 1)\right)}{\kappa_n I_{r\tau}} \tag{1.12}$$

As in equation (1.10), we can form an estimate of the peak voltage that the membrane reaches:

$$V_{m\_peak} = V_{rest} + \frac{I_{ex} + I_{rslope}}{C_m} t_r \tag{1.13}$$

We can see that V_{mem} now rises at a faster rate for a longer period of time than in equation (1.10). Under these conditions, V_{mem} easily exceeds threshold before V_r increases enough to compensate. Regardless of the actual time course of I_{ex}, the response of the neuron to excitatory inputs during this time window is facilitated over the normal condition.

Once the rising portion of the rebound ends, V_{mem} begins to fall and V_r continues to rise until $I_{r\tau}$ is balanced by the current in M2. Once this point is reached, V_r begins to fall, following V_m quickly. Both voltages return to their equilibrium value with no ringing, due to the fast downward action of the source follower, and the fact that M1 cannot drive V_{mem} below V_{rest}.

2.4 Excitatory Synapse

In response to spikes from returning echoes, the excitatory synapse drives and exponentially decaying current into the membrane dynamics circuit, which is given by:

$$I_{ex}(t) = I_{max} e^{\frac{-\kappa_p I_{ex\tau}}{C_{ex}} t} \tag{1.14}$$

Where I_{max} is set by the bias voltage, V_{exmax}.

2.5 Chip Performance

Membrane voltage traces in response different pulse-echo delays are shown in Figure 3. Tuning curves for the 13-neuron array are shown in Figure 4. Long-delay neurons are biased to have wider tuning curves than short-delay neurons using $I_{ex\tau}$.

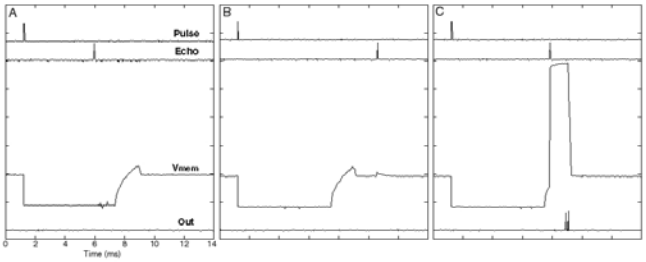

Figure 3. Response of a silicon delay-tuned neuron to artificial stimuli at different delays. Top trace is the spike representing an outgoing pulse. Second trace is a spike representing an echo. Third trace is V_{mem} of the neuron. Bottom trace shows output spikes from the neuron.

The entire 13-neuron array with biasing circuitry measures 927x390 μm in the AMI 1.5 μm process. A large portion of the layout size is due to capacitors that will be significantly reduced in future designs. Direct measurement of power consumption was not possible, due to additional testing circuits on chip with shared biasing, but simulations indicate that quiescent power consumption is on the order of 4mW and for computation of a period of 20ms with multiple echoes, average power consumption is around 2mW.

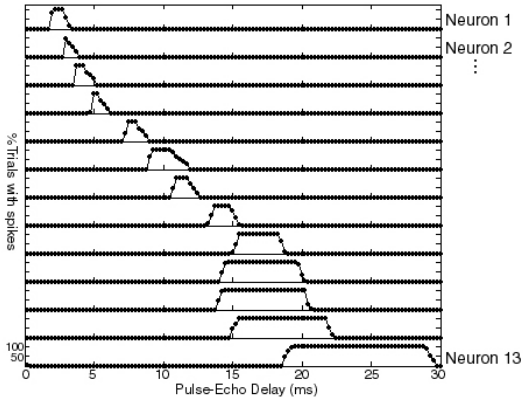

Figure 4. Example tuning curves for the 13-neuron array. Each neuron was presented with 100 pulse-echo spike pairs at delays ranging from 0 to 30ms in .25 ms intervals. Percent of trials on which the neuron spiked are plotted vs. time. (The peak in each plot reaches 100%)

3. SUMMARY

Neuromorphic VLSI design strives to capture the essential elements of any specific instance of neural computation and produce a circuit that will not only reproduce behavior in normal ecological conditions, but will react in qualitatively similar ways to damage and extreme stimulus conditions. The primary purpose is to test these neural algorithms in closed-loop, real-world conditions.

In this paper we present the design of an analog VLSI circuit that mimics the behavior of delay-tuned neurons in the bat midbrain. The circuit produces the delay-tuned responses by implementing the PIR model supported by numerous neurophysiological and anatomical studies. We have incorporated this chip into an artificial bat echolocation system to test these neurons in the closed-loop behavior of reporting target range and modifying parameters in response to a moving target.

This silicon implementation of the delay-tuned neurons of the bat provides a biologically realistic input layer for more detailed neural processing of target range such as attentional tracking and feature binding. While only a small piece of the sophisticated bat echolocation system, these circuits are a critical gateway for processing of range-related information.

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