# A Time-Series Processor for Sonar Mapping and Novelty Detection

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## ABSTRACT

A time-series processor chip, intended for sonar mapping and novelty detection applications, has been designed, fabricated and tested. The chip, when coupled with a sonar bearing and range estimation unit, receives an image of the environment as a voltage waveform. The bearing of an object is given by the magnitude of the signal, while its range is given by its time following the transmission of the sonar 'ping'. The chip stores this voltage waveform in a bank of sample-and-hold (S/H) elements and compares it to a previously stored trace. Objects that move in either azimuth or range are immediately detected and reported. The chip contains 54 S/H elements that are triggered by an on-board timer. The change detector can detect motion in bearing and range of 10 degrees/s and 11 cm/s, respectively. The maximum range is approximately 5m. Operating in the CMOS subthreshold region of operation, the novelty detection chip is designed for ultra-low power and micro-footprint smart surveillance systems. Implemented in a CMOS 0.5um process, it consumes less than 20 uW @ 8 Hz repetition rate (and less than 6 uW quiescent) with a 3V supply and occupies less than 0.3 sq. mm.

## 1. INTRODUCTION

The real-time processing of time domain, analog or digital, signals is required in many fields. This is particularly true for sonar data conditioning and understanding, where the received data has a pseudo-transient nature and is episodically distributed in time. Furthermore, active sensing with sonar is typically used to control behaving systems, e.g. robot navigation, or make real-time decisions, e.g. movement detection, which emphasizes the need for real-time, on-line and continuous time signal processing. Hence, working with time domain signals, analysis can be performed during signal acquisition, which leads to decisions and control with minimum latency.

Time series processing VLSI chips have been implemented primarily for two applications. The most common application is speech or transient acoustic signal classification [1],[2]. The second application is for sonar signal analysis [3]-[6]. In the former, the processor performs signal conditioning, storing and classification/identification based on well-known algorithms, such as Vector Quantization [1] and other correlation-based template matching schemes. In the case of the sonar signal analysis, the time-series processors are typically used to precondition sonar returns, i.e. filter, and digitize for output, such that standard digital computation hardware, e.g. DSPs, can be used to implement mapping and tracking algorithms [3],[4]. In rare cases, the chip may include some form of classification, e.g. coded "ping" identification, and output digitization [5]. This allows the system to distinguish between its own returns and those from other sources (on the same frequency).

On the other hand, we are working towards a self-contained chip that includes bearing and range estimation, mapping, storage and change/novelty detection. All computation will be performed with custom mixed-signal VLSI circuits. The architecture for the bearing and range estimation chip is presented in [6]. This paper focuses on the circuits and measurement results for mapping, storage and change/novelty detection. The two systems will eventually be merged into a single chip.

## 2. SYSTEM ARCHITECTURE

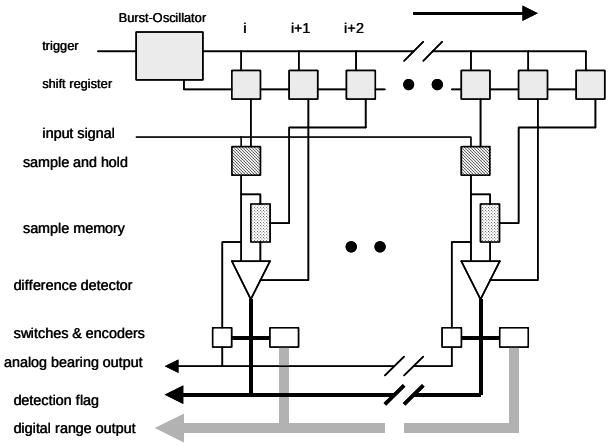


**Figure 1.** A block diagram of the time-series novelty detection chip. Upon receiving a trigger signal, the burst-oscillator begins driving a single bit down the shift register. The sample-and-hold unit *i* is activated by shift register (*SR*) unit *i*, the difference-detector unit *i* is activated by *SR(i+1)*, and the sample-memory transfer circuit *i* is activated by *SR(i+2)*. Likewise, the detection unit at position *i+1* (not shown) receives signals from SR units *i+1*, *i+2*, and *i+3*. The chip contains 54 S/H units

and 56 shift register units. The chip completely powers down once the bit leaves the shift register.

## 2.1 Block Diagram

Figure 1 shows the block diagram of the system. For normal operation, there are two inputs: the trigger and input signals. In our sonar application, an external source initiates the sonar ping and triggers the chip to begin sampling the returning echoes. The intended input to the chip is a real-time computed bearing angle, represented as a voltage, and range, encoded the time delay of the return relative to the sonar "ping". Any signal based on the returning sonar echo, however, can be used.

Following a trigger, the analog input signal is sampled (and recorded) at approximately 1.5 KHz for about 38 msec to an accuracy of about 16 mV. Any change in the sampled values since the last scan (above a threshold) produces output signals that indicate at what range and bearing it occurred.

## 2.2 Circuits

The primary goals in the design process were to minimize power consumption yet retain the precision needed for the change detection process. As a result, the design centered around using a digital shift register that would power the analog circuits up and down in a wave as they were needed in sequence. Each location in the array analyzes a specific interval of time following the trigger. Since the system only operates with a low duty cycle, (In our example, ~25% or less.) the on-board clock shuts down after the sampling period to save power.

*Sample and Hold Circuit*

The sample and hold circuit (Figure 2) is a transmission gate that connects the input line to a 210fF inter-poly capacitor using small transistor sizes (W/L=1.5um / 0.75um) to minimize offset problems from gate-capacitance-induced charge injection. The sampling capacitor was kept small to minimize the time and current required to charge it.

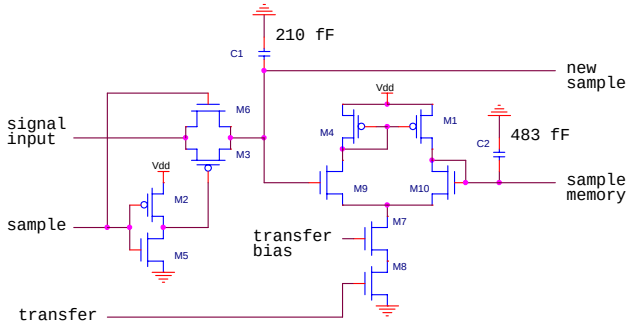


**Figure 2.** Sample-and-hold and memory transfer circuits. The digital sample signal connects the signal input to the 'new sample' capacitor. After the comparison (2 clock cycles later), the digital transfer signal copies the value into the sample memory capacitor.

*Burst Oscillator and Single Bit Shift Register*

The burst oscillator (Figure 3) is designed to begin producing a 50% duty-cycle square-wave output upon receiving a trigger signal that will continue oscillating until the bit traveling down the shift register 'pops' out the end. The oscillator is based on two inverters coupled by a simple RC-like circuit to set the oscillation frequency. When the burstrun signal is high, the transconductance amplifier-follower acts like a resistance, its output current saturating for large voltage differences. The effective resistance is controlled by the bias voltage oscbias. When 'burstrun' is low, the follower is powered down and the oscillator is clamped into a known state, reducing power.

There are two concerns about this circuit, high power consumption and frequency stability. High power consumption in the first inverter is an issue because the input voltage moves up and down around the threshold voltage where the current is highest. Frequency stability is a concern due to the strong dependence of the bias current on the oscbias voltage and on temperature. On the other hand, by modifying oscbias in a controlled way, the sampling rate of the system can be changed so that data can be stored/processed with variable temporal acuity. For the sonar application, this feature allows us to interrogate particular locations with higher range resolution.

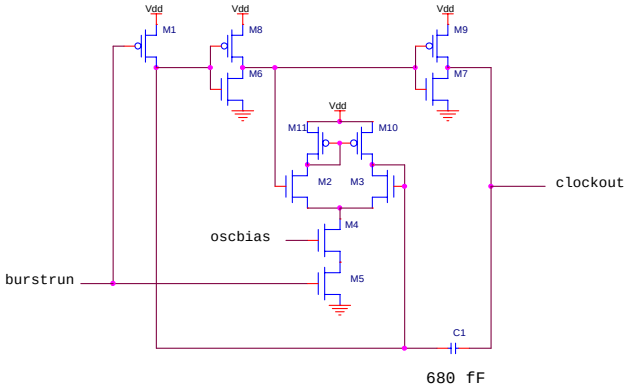


**Figure 3**. The on-board oscillator circuit.

*Difference Detection Circuit*

The difference detection circuit (Figure 4) is based on a transconductance amplifier followed by a current-mode full-wave rectifier. The resulting current is compared against a threshold current and the result is a digital voltage signal. The transconductance amplifier is activated by the output from shift register unit *i+1*, in the clock cycle following sampling.

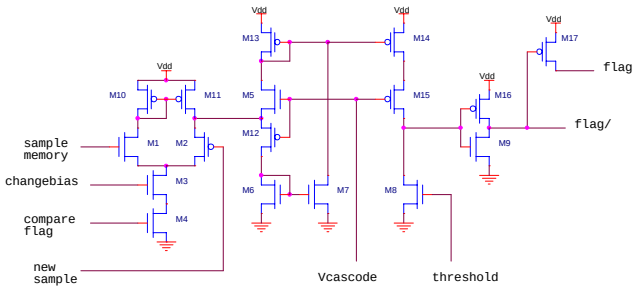


**Figure 4**. The difference detection circuit.

The transconductance amplifier operating in subthreshold has an input dynamic range of about +/- 100 mV. The sensitivity of this circuit to differential input voltage is dependent on the bias current, the threshold current, and (at the highest sensitivity settings,) the drain conductance of the current comparison transistors (M15 and M8). For this reason, the pFET mirror has been cascoded. For power conservation, when 'compare flag' is low, there is no quiescent current in this circuit.

*Bearing and Range Outputs*

Upon detecting a change, the flag/ signal (Figure 4) is pulled low, activating a wired-OR pull-up transistor to indicate the detection off-chip. This signal also locally activates two other circuits, the analog 'bearing output' and a digital 'range address' bus. The flag/ signal turns on a voltage-follower circuit to drive the newly sampled value off-chip, signaling the ('bearing') value that triggered the detection event. The flag/ signal also drives a 6-bit binary encoder to indicate which element is signaling the event. These circuits are not shown.

*Memory Transfer Circuit*

Once the comparison between old and new values has been performed, the output from shift register unit *i+2* is used to turn on a follower circuit (Figure 2) driving the memory capacitor voltage to the sampled voltage level. The sample memory capacitor needed to be large enough to minimize voltage loss, but kept small to minimize the current needed to charge it. A 483fF capacitor was chosen based on estimates from simulation.

## 3. CHIP TESTING

*The Triggered Sample-and-Hold Subsystem*

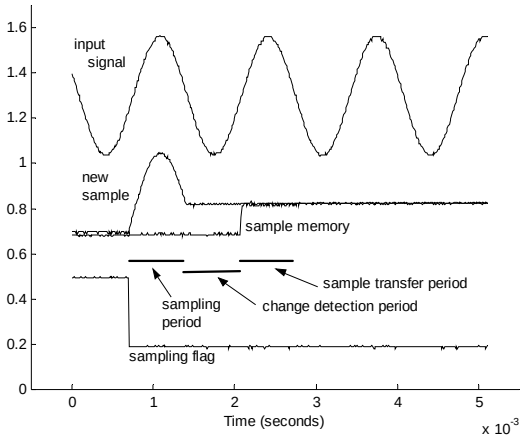


**Figure 5**. A test of the sample-and-hold circuit (tap #1) shows the 'new sample' and 'sample memory' voltages. Processing at each pixel occurs in three stages: sampling of the input signal, comparison to the stored previous value and transfer of the new value to the memory location. The input signal trace has been voltage shifted and the sampling flag voltage has been rescaled to fit in the figure.

The sample and hold circuit for tap #1 is shown operating in Figure 5. A 500 mV p-p sinewave is the input signal, showing the S/H capacitor following the input during the sampling period. The input value at the close of the unit sample period is the stored value. At the end of the change detection period, the new sample is transferred to the sample memory capacitor.

The memory transfer circuit produces a slight systematic offset of about -10 mV due to the parasitic gate-source capacitance between the sampling capacitor and the common node of the differential pair. The 483fF storage capacitor has been tested and shown to lose voltage approximately linearly at 6.1mV / second in the dark (at room temperature).

*The Difference Detection and Bearing Reporting Subsystem*

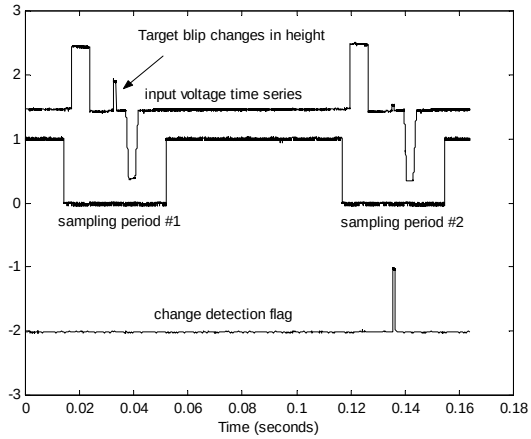


**Figure 6**. Demonstration of amplitude change detection. In this example, a moveable "blip" (middle feature) is changed in amplitude (-60 mV). The change detection flag indicates the change one internal clock cycle following the new sample.

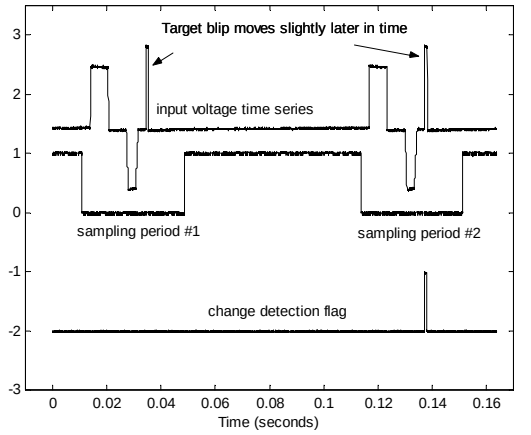


**Figure 7**. Demonstration of range change detection. In this example, a static background pattern is played to the chip (first two features) and a moveable "blip" is moved slightly later in time between the two sampling periods. In this case, only 40 usec was needed for the blip to cross into a new detection unit (change detected).

The difference detection circuits were tested by repeatedly presenting an input waveform and modifying only one part of the stimulus (narrow 'blip') in either amplitude (Figure 6) or occurrence in time (which produces changes in amplitude) (Figure 7). The change detection threshold was set to prevent detection in the static input case.

Random offsets in the S/H, memory transfer, and change detection circuits produced shifts in the detection threshold of individual circuits. Systematic (e.g., memory leakage) and random offsets (e.g., comparator input offsets) produce a direction asymmetry in the detection threshold; For example, a positive offset will reduce the minimum rise and increase the minimum drop needed to trigger the unit.

*Change-Triggered Bearing/Range Output*

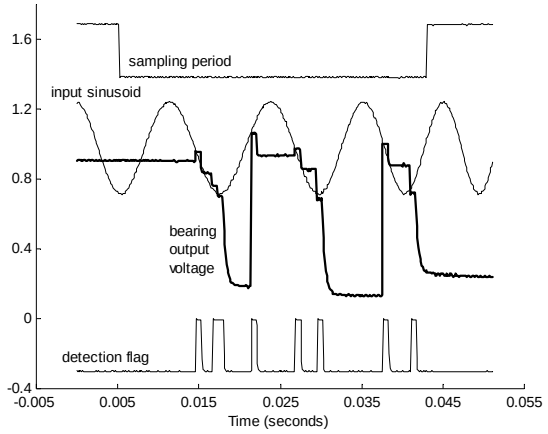


**Figure 8**. Demonstration of the bearing output signal.

Upon detecting a difference between the newly received sample and the previously stored value (in our sonar example, this will represent the 'target bearing'), the detection signal turns on a follower circuit that drives the newly sample voltage off-chip on a common analog line. Figure 8 shows an example where an unsynchronized FM sweep triggers many change detection events, and the bearing output voltage jumps to report the latest sample at the location of the change..

*Power Consumption*

There are several modes in which the power consumption is relevant. Reading the analog bearing voltage (and other test points in the circuit) requires biasing large follower circuits to drive the pads quickly. In this mode, quiescent power consumption of the circuit (no triggering of the sample-and-hold system) is at about (1.8uA x 3v) 5.4uW. When triggered at an 8 Hz repetition rate (with 32 ms sampling time) the power consumption rises to (6.2uA x 3v) 18.6uW.

If, however, the detection flag and the digital range output are sufficient as a wake-up signal for other systems, at an 8 Hz repetition rate and with no change detection events, a power of (2uA x 3v) 6uW is measured. In the quiescent mode (no bearing output, and no sampling), the system now draws (335nA x 3v) 1uW. Note that these measurements do not include the power required to generate the seven bias voltages needed to operate the chip.

### 3.1 Sonar System Integration and the Future

This chip was designed for sonar-derived target *bearing* inputs (as part of a larger research project [6]), however, the circuit operates on any repetitive event-triggered voltage time-series. We have integrated this chip with an acoustic sonar front-end [7] using echo amplitude signals (instead of bearing) to drive the input to the chip.

A number of improvements are planned, particularly in the area of power consumption, offset errors, and operational flexibility. A new, low-power oscillator circuit is planned, an even lower offset S/H circuit (smaller input transistors for the memory transfer circuit), and lower-offset difference detection circuits (larger transistors) are planned.

## 4. SUMMARY

We have designed, fabricated, and tested a low power time-series novelty detector chip intended for use in a sonar application, but easily applicable to other problems. Following an input trigger signal this chip records samples from the incoming signal and compares them to previously recorded values at the same relative time from the trigger. We have integrated this chip into a functioning acoustic sonar system to investigate its detection capabilities. The architecture has been chosen to reduce power consumption by asynchronously activating circuits only when they are needed.

## 5. ACKNOWLEDGEMENTS

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