A LOW-POWER CMOS NEURAL AMPLIFIER WITH AMPLITUDE MEASUREMENTS FOR SPIKE SORTING

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ABSTRACT

Integrated, low-power, low-noise CMOS neural amplifiers have recently grown in importance as large microelectrode arrays have begun to be practical. With an eye to a future where thousands of signals must be transmitted over a limited bandwidth link or be processed *in situ*, we are developing low-power neural amplifiers with integrated pre-filtering and measurements of the spike signal to facilitate spike-sorting and data reduction prior to transmission to a data-acquisition system. We have fabricated a prototype circuit in a commercially-available 1.5μm, 2-metal, 2-poly CMOS process that occupies approximately 91,000 square μm. We report circuit characteristics for a 1.5V power supply, suitable for single cell battery operation. In one specific configuration, the circuit bandpass filters the incoming signal from 22Hz to 6.7kHz while providing a gain of 42.5dB. With an amplifier power consumption of 0.8 μW, the rms input-referred noise is 20.6μV.

1. INTRODUCTION

Neural recording from large microelectrode arrays is becoming routine in many neurophysiology laboratories around the world. The recording and signal processing of this massive torrent of analog data, however, remains a challenge, especially when the experimental subjects are small, mobile animals. While existing systems utilize large bundles of wires and banks of high-speed digital signal processing (DSP) boards running spike-sorting software, this is not a scalable solution for obtaining ensemble neural data from animals in flight or for implanted neural prosthetics.

To support the future of autonomous neural ensemble recordings, we are developing low-power VLSI processors for integrated spike-sorting at or near individual electrodes. The massive reduction of data possible with successful spike-sorting is appropriate to reduce the power needed for transmission of spike data.

Integrated biosignal amplifiers have been designed by many other investigators under different constraints such as low-noise, low-frequency, low-power, low-voltage, zero-DC gain, and in combinations (e.g., [1-9]). Much of our design is defined by the effort to operate on a single cell battery (1.5V); this is an important strategy for reducing system weight. The use of CMOS transistors in or near the subthreshold region of operation provides us with lower gate-to-source voltages, and a drain-source saturation voltage of about 100mV.

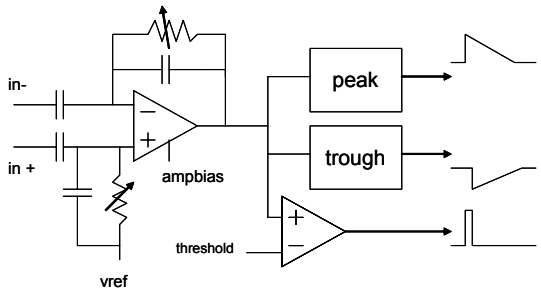

Figure 1. Block diagram of the neural amplifier information flow and basic function.

2. SYSTEM DESIGN

2.1 Design Approach

A block diagram of system components is shown in Figure 1. The input consists of differential electrode inputs and the outputs are from: an amplifier, a peak detector, a trough detector, and a level detector.

The design of the neural amplifier is based on a capacitive feedback approach as described by Harrison and Charles [1] with a weakly-biased nFET as a variable resistive element. This approach allows us to vary the high-pass filter corner frequency to reduce 60 Hz noise and to limit the low-frequency noise contribution. Following the amplifier, we have implemented a peak detector, a trough detector, and a level detector in order to measure the amplitude of the spike signal and facilitate the sorting of spikes.

2.2 Prefiltering and Amplification

The amplifier (shown in Fig. 2) was designed to provide 40dB of voltage gain using a capacitor divider which compensated for expected parasitic capacitances. This design capacitively couples the differential inputs to allow the rejection of expected DC potential differences between the sensing electrode and the reference electrode. The two inputs to the transconductance amplifier would be floating nodes except that two nFET transistors are used as variable resistors (set by *rbias*) to control

the common-mode voltage (*vref*) and the high-pass corner frequency (-3dB).

The midband gain is (C1 / C2), the low-frequency corner is: $f_{LF} \approx \frac{1}{2\pi \cdot r \cdot C2}$, and the high-frequency corner is given by: $f_{HF} \approx \frac{G_m C2}{2\pi(C1+C2)\left(C1+C_L\right)}$ where C_L is the load capacitance and G_m is the transconductance of the differential amplifier (determined by *ampbias*). Unless otherwise noted, all transistors shown were fabricated using W=4.8μm and L=4.8μm.

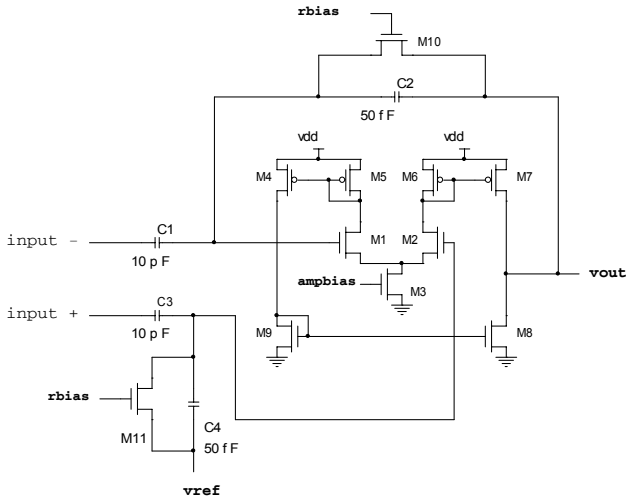

Figure 2. Schematic of the differential amplifier with capacitive divider feedback to provide a differential voltage gain of 40dB. Capacitor values are chosen to compensate for expected parasitic capacitances. The transconductance amplifier bias is controlled by *ampbias* which sets the high-frequency rolloff frequency.

2.3 Peak-to-Trough Difference

As a first step towards the development of an automatic spike-sorting system, we have integrated a peak and trough measurement (Figs 3 and 4) to extract information about spike amplitude. As a first step, we utilize the observation that the peak-to-trough difference is one of the most useful features for spike sorting [10]. These simple zero-offset peak detector (and trough detector) circuits are designed to operate on 1.5V supply voltages and comprise transconductance amplifiers with negative feedback around MOS transistors.

In the case of the peak-detector, the amplifier output needs to be higher than the input by the gate-source voltage of M4, so a simple transconductance amplifier suffices. In order to keep the differential-pair bias transistor saturated, the common-mode voltage (*vref*) must remain higher than about 0.8V, precluding the use of a simpler p-type transconductance amplifier for the trough-detector. For the trough-detector, the amplifier output needs to be lower than the input by the gate-source voltage of M10, thus a wide-output-range transconductance amplifier was used.

Small transistors were used for the rectifier element to reduce the gate to source capacitance and to minimize the capacitive load on the transconductance amplifier.

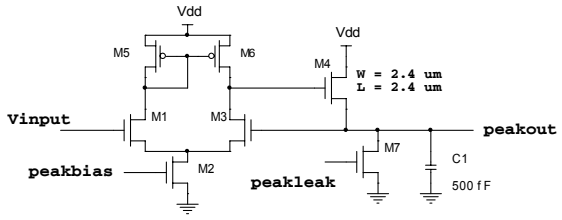

Figure 3. Zero-offset peak detector with a variable leak set by *peakleak*.

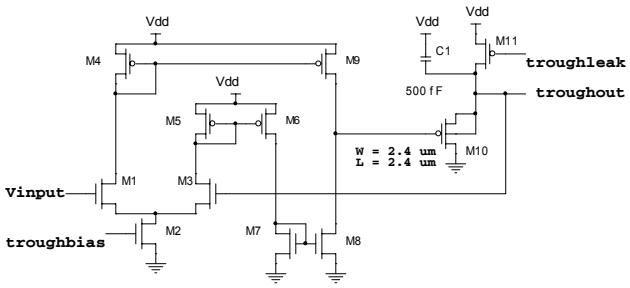

Figure 4. Zero-offset trough circuit with a variable leak set by *troughleak*.

The detection of spike time is performed with a simple level detector shown in Fig. 5. This digital output provides a time reference for sampling the peak and trough detector outputs.

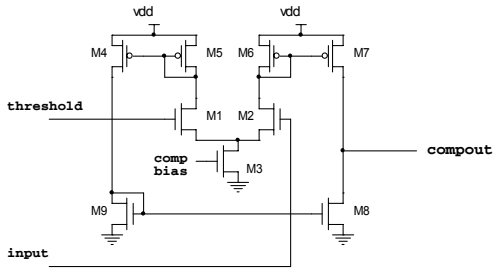

Figure 5. Level detector circuit used to detect the occurrence of spikes using a simple threshold.

3. CHIP MEASUREMENTS

The circuit layout occupies about 91,000 μm^2, dominated by the two 10pF capacitors. The chip was fabricated in a 1.5μm double-poly, double-metal process. All data shown are obtained with Vdd = 1.5V.

3.1 Frequency Response and Gain

Although we designed the amplifier for a gain of 40dB, we measure a midband voltage gain of approximately 42.5dB (gain = 133). Independent control of the low-frequency corner using *rbias* and the high-frequency corner using *ampbias* was confirmed and is shown in Figs. 6 and 7.

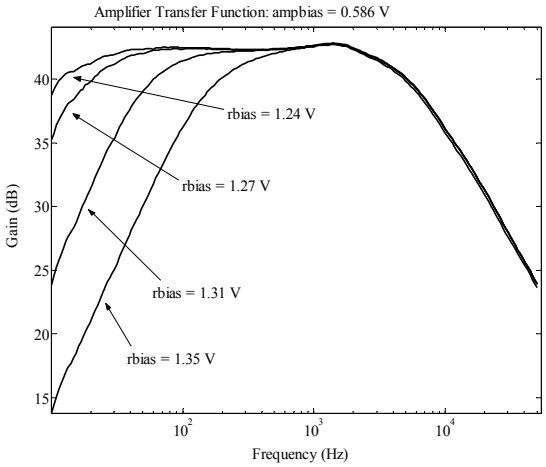

Figure 6. Frequency response of the amplifier as *rbias* is changed, leaving *ampbias* fixed at 0.586V. The parameter *rbias* controls the low-frequency corner of the bandpass filter, making it possible to filter out some of the 60 Hz interference present in any recording situation.

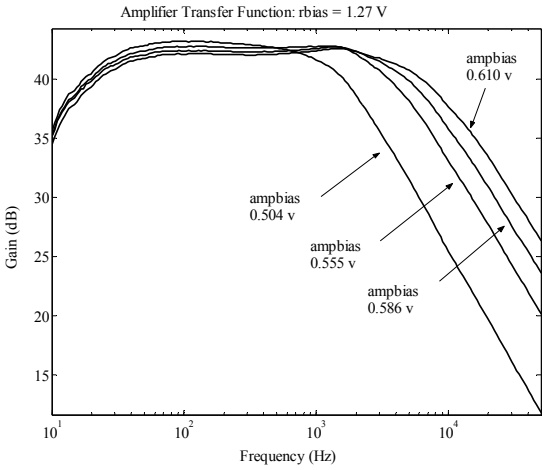

Figure 7. Frequency response of the amplifier as ampbias is changed, leaving rbias fixed at 1.27V. The parameter ampbias controls the high-frequency corner of the bandpass filter.

Using the parameters: *ampbias*=0.610V and *rbias*=1.27V, the corner frequencies of the bandpass response (-3dB frequencies) occur at 22Hz and 6.7kHz. Using *ampbias* = 0.620V and *rbias* = 1.35V, the corner frequencies occur at 182Hz and 9kHz.

3.2 Power and Noise

Power consumption in the amplifier depends on the bias condition determined by the parameter *ampbias*. With *ampbias* = 0.610V the power was measured to be 0.8 μW and with *ampbias* = 0.620V was measured to be 1.0 μW. We also measured the noise spectral density at the output of the amplifier and computed the input-referred values by dividing each noise measurement by the measured gain at the closest measured frequency (Figure 8). By integrating under the noise spectral density curve from 10Hz to 10kHz we obtain a total input-referred rms noise voltage of 20.6μV rms, again with *ampbias*=0.610V and *rbias*=1.27V.

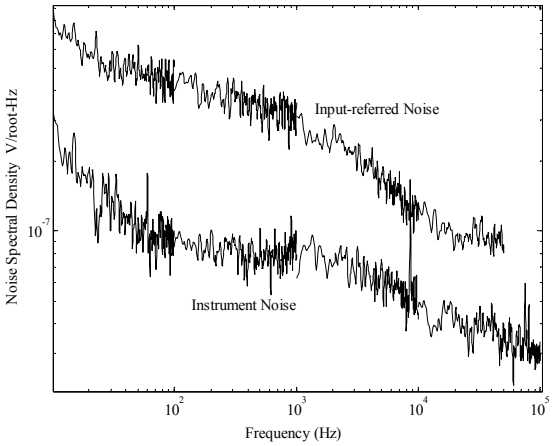

Figure 8. Noise spectral density for the neural amplifier with parameters: *ampbias* = 0.610V and *rbias* = 1.27V. The input-referred noise is computed from the measured output noise spectrum divided by the measured gain at the closest measured frequency.

3.3 Peak-to-Trough Measurement

We have tested the peak and trough detector circuits with pre-recorded ferret cortex recordings obtained from the Neural Systems Laboratory at the University of Maryland to evaluate their function with realistic signals. An arbitrary-waveform generator with an attenuator supplies signals to the input of the amplifier. Figure 9 shows an example output spike and the resulting response from peak and trough circuits. While not shown in the example, the decay rates need not remain constant and can be strobed high following a spike to reset the detectors.

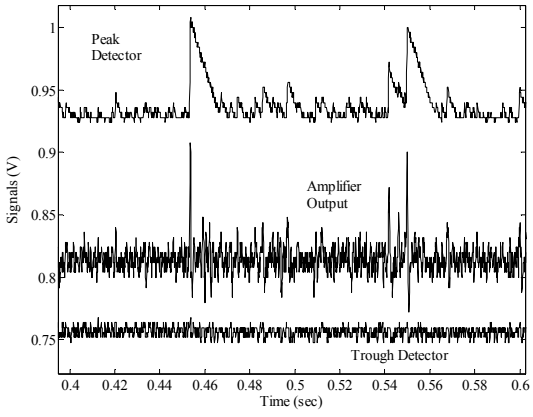

Figure 9. Peak and trough detectors (top and bottom) respond to a spike input. The peak detector output has been shifted upwards by 120mV and the trough detector

downwards by 40mV for clarity. In this example, the decay of the peak detector is ~2.5V/s and the decay rate of the trough circuit has been set to be small.

3.4 Neural Spikes and Sorting

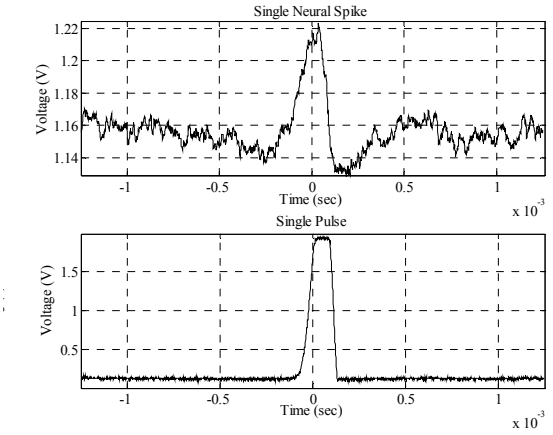

Figure 10. The level detector output indicates when the analog signal exceeds a threshold. This signal is used to trigger the sampling of the peak and trough values for spike-sorting.

We present pre-recorded ferret cortical spikes to the chip and measure the response. Using the level detector output (Figure 10) the peak and trough detectors were sampled. Figure 11 shows the signal, detected spikes, and a histogram of spike amplitudes.

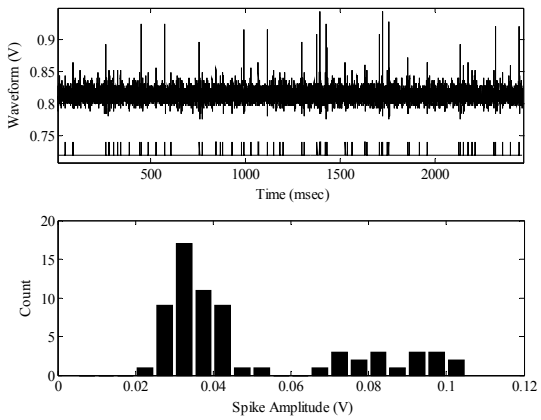

Figure 11. Responses to pre-recorded ferret cortical spikes: (top panel: upper trace) amplifier output, (top panel: bottom trace) scaled level detector output (bottom panel) histogram of spike amplitudes showing at least two classes of spikes based on amplitude discrimination alone.

4. SUMMARY

We have designed, fabricated, and tested a low-power neural amplifier suitable for use in neural recordings, incorporating appropriate filtering and the initial stages of feature extraction useful for subsequent spike-sorting. While the noise level seen in this implementation is high compared to other designs which use considerably more power, it is acceptable for our beginning efforts and we are working to lower it further.

5. ACKNOWLEDGEMENTS

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