LINEAR CURRENT MODE IMAGER WITH LOW FIX PATTERN NOISE

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ABSTRACT

A new imaging architecture with linear current mode active pixel sensor (APS) is presented. Focal plane image processing in the current domain includes correlated double sampling (CDS) unit for fixed pattern noise (FPN) suppression. The CDS unit is composed of first generation current conveyer circuit and class AB cascaded current memory cell. Measured FPN of 0.9% from saturation level is achieved with the CDS unit compared to 1.9% FPN from current mode images without noise suppression circuitry. A 40 by 40 imaging array was fabricated in a standard 0.5µm process and its functionality was successfully tested. Theoretical analysis for second order non-linear effects is also presented.

1. INTRODUCTION

Current mode active pixel sensors (APS) have provided a new avenue of research for focal plane image processing architectures [1-6]. Current mode APS provide certain advantages over traditional voltage mode APS. These advantages are: higher read out bandwidth and easier incorporation of analog computation units necessary for image processing, such as convolution [2,3], image reconstruction and compression [4]. The constant voltage on the read out lines requires no (dis)charging time when a pixel photocurrent is read out of the imaging array. Hence, high scan out rates can be achieved with current mode APS. Arithmetic operations, such as additions, subtractions and scalar multiplications, are trivially implemented in the current domain [6]. More complicated switch current circuits, such as ADCs[5], ratio current circuit and others, are also extensively covered in the literature[7,8], extending the library of available processing elements for focal plane image processing.

The main disadvantage of current mode processing is low precession due to the noisy nature of these circuits. Current mode imaging architectures have reported much higher fix pattern noise (FPN) figure compared to their voltage mode rivals [9]. Typical non-linear photocurrent outputs have limited the effectiveness of noise suppression circuitry [5] and limit the functionality of these imagers.

In this paper, we describe a new linear current mode imaging architecture. The linear photocurrent allows for easy integration of a current mode CDS unit, which improves the noise characteristics of this system. In section two, we describe the main components of the system and their functionality. Experimental results and theoretical models for second order non-linear effects of the system are discussed in section three. Conclusions are drawn in section four.

2. SYSTEM OVERVIEW

2.1 General Overview

The two main components of the system are the linear photo pixel and the correlated double sampling (CDS) unit. An array of 40 by 40 photo detectors is designed in a standard 0.5µm 3M1P CMOS process. The digital scanning registers surrounding the photo array control the integration time of the photo pixels and address a single pixel of the photo array at one time instance. Once a pixel is addressed, both integrated and reset photocurrents are presented to the CDS unit in a sequential manner. A single CDS unit is used for the entire imager, eliminating mismatches that can be introduced when multiple (column) CDS units are implemented. The CDS unit is operated in two phases. During the first phase of operation, the integrated photo current is stored in the current memory cell of the CDS unit. This current is subtracted from the reset current during the second phase of operation and the corrected photocurrent is presented outside the chip. Hence, the CDS unit eliminates the photo current threshold variations of the pixel read out transistor and it also eliminates kTC and 1/f noise of the pixel. The corrected photocurrent can easily be used as an input to various switch current processing units, such as current mode ADCs [5] and/or analog convolution processors [6], where the accuracy of the final result can be improved due to the improved accuracy of the input photocurrent.

2.2 Linear Photo pixel

The photo pixel is composed of three PMOS transistors (M1-M3) and a photodiode implemented as n-based diffusion over p-based substrate (figure 1). The reset transistor M1 controls the operating mode of the photodiode. When the gate of transistor M1 is pulled down to V_{ss}, this transistor is turned on and the photo diode is charged to its maximum voltage V_{reset}. The different supply voltage of transistor M1, allows an easy manipulation of the operating range of the photodiode and therefore it controls the upper bound of the gate voltage swing of transistor M2. When the gate of transistor M1 is pulled up to V_{reset}, the reset transistor is turned off and the floating reversed biased photodiode is discharged at a rate proportional to the optical excitation of the pixel's active area.

Transistor M2 acts as a transimpedance amplifier, converting and amplifying the photodiode voltage into an output current. The output of the transimpedance amplifier is connected to a virtual ground circuit via pixel switch transistors M3 and column switch transistor M4. The virtual ground (VG) circuit is the first stage of the CDS unit and a single unit is used for the entire imaging array. The VG circuit is composed of two current conveyers connected in a negative feedback, pinning the input node potential V_{in} to the reference potential V_{ref}. Hence, the drain potential of transistor M2 is fixed to the V_{ref} potential, which is biased externally. The unselected column lines of the imager are connected directly to V_{ref} , keeping all bus lines charged to the same potential.

Transimpedance amplifier M2 can be operated in the triode region, where linear photo voltage to current conversion is ensured. In order to operate transistor M2 in the triode region, two criteria must be satisfied. First, a minimal voltage drop between the drain and source of M2 is required in order for an output current to flow through this transistor. Therefore, V_{ref} can have a maximum value of V_{dd}-Δ, where Δ is approximately 0.2V. Second, V_{reset} must be at least one threshold voltage (V_t) bellow V_{ref}. This criterion ensures the voltage at the gate of M2 is always V_t bellow the drain voltage of M2. Since, the gate voltage will decrease with optical excitation of the photodiode, transistor M2 will always operate in the linear mode. Hence, the transimpedance amplifier M2 will output a current linearly

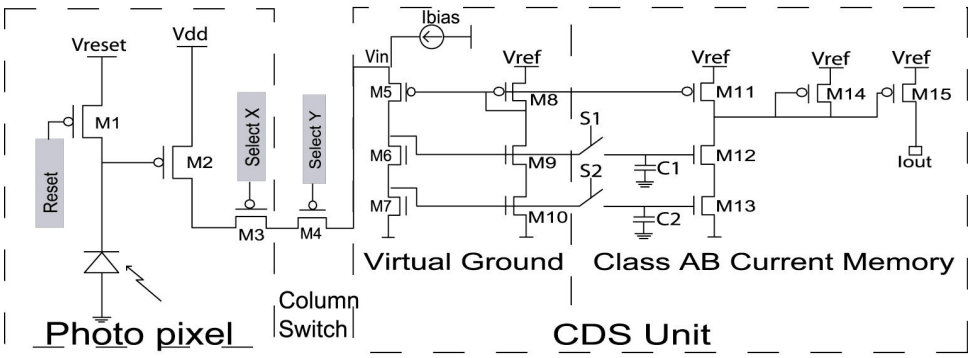

Figure 1: System Overview – pixel circuitry, column switches and CDS unit

correlated with optical excitation and it will be described by equation (1).

$$I_{out} = \mu_p C_{OX} \frac{W}{L}[(V_{photo} - V_t)V_{ref} - \frac{V_{ref}^2}{2}] \quad (1)$$

where μ_p is hole mobility, C_{OX} is oxide capacitance, V_{photo} is the photo voltage of the photodiode which effectively appears as $V_{gs,M2}$, and V_{ref} is the reference voltage of the virtual ground which is equivalent to $V_{ds,M2}$.

2.3 CDS Unit

The functionality of the CDS unit is to remove photo current threshold variations of the pixel read out transistor and also to eliminate kTC and 1/f noise of the photodiode. The two components of the CDS unit are: the virtual ground circuit and the current memory cell. The cascode current mirror, composed of transistors M6, M7, M9 and M10, sets the currents through both branches of the virtual ground circuit (M5-M7 and M8-M19 transistor branch) to be equal. The second current mirror in the virtual ground, which is composed of transistors M5 and M8, will provide equal currents in both branches only if the source voltages of these transistors are the same. Since the bottom current mirror already sets equal currents in both branches of the VG circuit, voltage V_{ref} and V_{in} must be at equal potentials.

The VG circuit is used to mask the large capacitance of the current buses. The impedance at the input of the VG circuit can be easily derived to be *~[1/gm(pfets)]*. Assuming a single pixel is selected per current output line, a quiescent pixel (dark) current of ~2.2μA flows (see figure 3) into the VG circuit, and the *W/L* of all the transistors is 10, giving an input impedance of ~300kΩ for this CMOS process. Larger photo currents will flow in the VG circuit as more light is absorbed, leading to smaller VG input impedance. Increasing the bias current I_{bias} will also decrease the input resistance. The line capacitance, primarily determined by the drain diffusion capacitance of the read-out switches, is ~2fF/pixel in a row or column. With 40 pixels on each row, the VG response time is 24ns. Hence, it is easy to obtain the required VG response time constant by increasing the I_{bias} current.

The memory cell in the CDS unit is implemented as class AB cascode current memory cell [8]. The memory unit is composed of transistors M12 and M13 together with capacitors C1 and C2 and switch transistors S1 and S2. During the read operation, switch transistors S1 and S2 are turn on and the mirrored current through M12 and M13 transistors sets the gate voltages of these transistors on capacitors C1 and C2. When switch transistors S1 and S2 are turned off, capacitors C1 and C2 keep the gate voltage of M12 and M13 at the same potential and they continue to sink the same current as the original current. During the first phase of operation of the CDS, switch S1 and S2 are turned on and the integrated photo current sets the voltages at the gate nodes of transistors M12 and M13. Implementing a cascaded memory cell minimizes channel length modulation effects, which are prominent when a single memory cell is used. After the completion of this phase, switch S1 and S2 are turned off and the pixel is reset at this time. Hence, transistor M11 sources a copy of the reset current and the final current output of the CDS will be the difference between the stored integrated photo current and the reset current. This output current is provided outside the chip via a diode connected transistor M14, whose purpose is to mirror the current flowing through the output branch of the CDS unit via M15 transistor.

One of the main limitations of the CDS circuit is the charge injection error due to the switch transistors S1 and S2. These charge injections are due to two factors. First, when switch transistor S1 and S2 are turned on, channel charge is accumulated under the gate of these transistors. When these transistors are turned off, the channel charge is removed through the source and drain of S1 and S2 transistors. Hence, some residual charge will be stored in C1 and C2 capacitors and this charge will be proportional to the current flowing through these transistors before the switching. The second limiting factor, is the clock feed through due to the overlap capacitance between the gate and source of S1 and S2 transistor. The charge injection effects are minimized by introducing dummy switches before and after the switch transistors and implanting large storage capacitors that satisfy the bandwidth requirements of the CDS circuit.

2.4 Circuit operation and limitations

Performing CDS in the current mode domain has been described previously in the literature [5]. The main draw back of these circuits is the non-linear photo current output, which limits the functionality of the CDS circuit. The primary functionality of a CDS circuit is to remove current or voltage offsets due to variations in the readout transistor of the photo pixel, in addition to canceling kTC and 1/f noise. These variations are easily cancelled when dealing with linear output (current or voltage) from the pixel. Hence, voltage mode CDS has been extensively explored in the literature due to the linear pixel voltage output, where voltage offset variations are corrected with a CDS circuit [9].

The linear current mode pixel allows for easy elimination of threshold variations of the output transimpedance amplifier M2. During the first phase of the CDS operation, a photo current I_{photo},

described by equation (1), set the potential on capacitors C1 and C2. When the pixel is reset, a reset current I_{reset} flows through M11 transistor described by equation (2):

$$I_{reset} = \mu_p C_{OX} \frac{W}{L}[(V_{reset} - V_t)V_{ref} - \frac{V_{ref}^2}{2}] \quad (2)$$

The final output of the CDS circuit is the difference between I_{photo} and I_{reset} and is given by equation [3].

$$I_{out} = I_{photo} - I_{reset} = \mu_p C_{OX} \frac{W}{L} V_{ref}(V_{reset} - V_{photo}) \quad (3)$$

The final current output I_{out} does not depend on the threshold voltage variations of M2 transistor and is linearly proportional to the photodiode voltage, V_{photo}. In order to maximize the output current of the CDS unit, Vref potential should be as high as possible to yield high gain.

3. RESULTS

3.1 Experimental Results

The imaging system described in Section 2 was fabricated and tested in a standard 0.5µm process. The linear response of the pixel output current over time under various reset potentials is measured and presented in figure 2. The illumination intensity is set to 50uW/cm^2 at 700nm wavelength (red spectrum) with I_{bias} of 1.8uA and V_{ref} of 4.6V. The pixel current output is increased linearly over time as more optical charge is collected on the photodiode. When the photodiode is reset at 3.7V, the output transimpedance amplifier is operated in a weak inversion mode and an exponential characteristic in the output current is observed. For smaller reset voltage value, the transimpedance amplifier is operated in the triode region and linear current output is observed. The saturation current is 2.77uA.

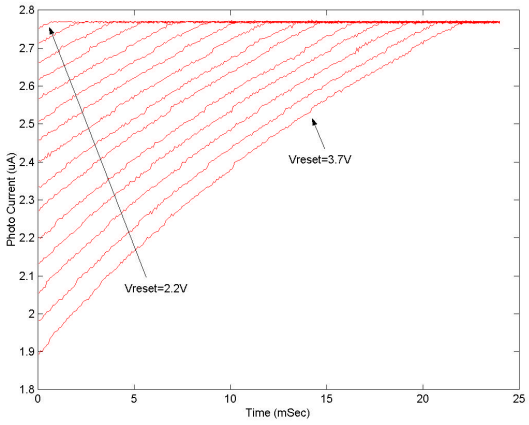

Figure 2: Linear current responses under various V_{reset} biases

The fixed pattern noise of the system is evaluated with and without the CDS unit. The fixed pattern noise with noise suppression circuitry is 0.8% of the saturation current. This error is primarily due to charge injection errors in the current memory cell and hole mobility dependence on the gate voltage of transistor M2, which is described in the next section. The fixed pattern noise without noise suppression circuit is 1.9% of saturation current and it is largely due to the threshold voltage variations of the transimpedance amplifier.

Real life images obtained with this imager are presented in figure 3, where the benefits of the current mode CDS are evident. The left image is obtained using noise correction circuit and it presents smaller variations between pixels with similar intensity. The image on the right is obtained without noise correction and variations between pixels with similar intensity are easily observed.

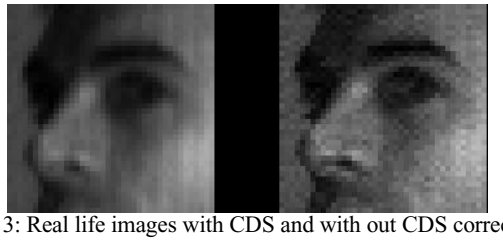

Figure 3: Real life images with CDS and with out CDS correction

3.2 Second order non linearity

During regular mode of operation (V_{reset}=3.0V), small non-linear effects in the output current are observed (figure 4). These non-linear effects are due to two factors: hole mobility dependence on the gate voltage in transistor M2 and non-linear photodiode voltage discharge. Three models were created in order to compare first and second order non-linear effects of the photo pixel. The linear fit model assumes linear current output as the photodiode voltage linearly discharges. This model assumes the behavior described by equation (1) and yields 10% error when compared to real data (figure 4). The second model incorporates hole mobility dependence on the gate voltage of M2 transistor and is described by equation (4)

$$\mu_p = \frac{\mu_0}{1 + U0(V_{gs} - V_t) + U1(V_{gs} - V_t)^2} \quad (4)$$

In equation (4), μ_0 is hole mobility in long channel transistor, while parameters U0 and U1 are used to model first and second order mobility dependence on the gate voltage in a short channel transistor. These values are extracted from a test transistor operating in a linear mode and they are calculated to be 0.245V^{-1} and 1.56E-3V^{-2}. Equation (4) is used to substitute hole mobility in equation (1). This model yields 2% error when compared to real data.

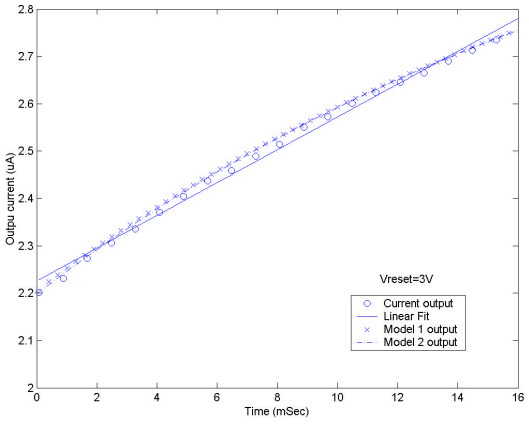

Figure 4: Linear current response and model data

The final model incorporates also non-linear voltage discharge characteristics of the photodiode. This model accounts

for the dynamic behavior of both depletion capacitance of the photodiode and non-linear photocurrent generation due to variable depletion lengths. Due to the discharge of the reverse biased diode, the depletion length of the diode will decrease. This will effectively increase the depletion capacitance of the photodiode. The photocurrent, which is composed of drift and diffusion current, will change accordingly with the change of the diffusion length. The diffusion components of the photocurrent will increase, while the drift component will decrease. This complex model also accounts for all parasitic capacitance at the photodiode node. This model yields less then 1% error when compared to real data measurements.

The main cause for non-linear current in this imaging architecture is the mobility dependence on the gate voltage of the output transimpedance amplifier. Using longer transistors can decrease these effects. The requirement for high pixel density and hence small pixel size will put an upper bound on the size of the transistors and on the precision of the output current. Linear degradation due to mobility dependence on the photodiode voltage is another draw back of the current mode pixels. Voltage mode APS use source follower as a read out transistor and hence they are immune to mobility degradations.

3.3 Chip characteristics

Summary of the chip characteristics is presented in Table 1. The maximum scanning rate is limited by the virtual ground circuit to 41MHz. Using 40x40 (1000x1000) pixel array, a frame rate of 25k (41) frames per second can be achieved. The low fix pattern noise (0.8% of saturation current) is comparable to voltage mode APS. The low power consumption of this system of 2mW is another advantage of current mode imaging systems.

Technology	0.5 µm Nwell CMOS
No. Transistors	10K
Array Size	40 x 40
Pixel Size	10 µm x 10 µm
Chip Size	1.5mm x 1,5mm
FPN with CDS	0.8% of sat. level
FPN with CDS	1.9% of sat. level
Dynamic Range	1 – 200 µW/cm^2
Frame Rate	30fps – 25000fps
Saturation level	2.77µA
Power Consumption Vdd=5V @ 50uW/cm^2	2mW

Table I: Chip characteristics.

4. CONCLUSION

A 40x40 photo array was designed and tested in 0.5µm CMOS process. The linear photo current allows for easy integration with noise suppression circuits. Noise suppression circuits are implemented in current mode domain, allowing for low power and small circuit area. This circuit can easily be used together with switch current circuits for focal plane image processing.

6. REFERENCES

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